**COA Project Part I: ISA Design**

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Word Length = 8 bits

Instruction Length = 16 bits

Registers = 4

***Instruction Format***:-

| Opcode | Register | Addressing mode | Immediate / Address / Register |
| --- | --- | --- | --- |
| 4 bits | 2 bits | 2 bits | 8 bits |

| Register | Binary Representation |
| --- | --- |
| R0 | 00 |
| R1 | 01 |
| R2 | 10 |
| R3 | 11 |

| Addressing mode | Binary Representation |
| --- | --- |
| Immediate | 00 |
| Register | 01 |
| Direct | 10 |

| Instruction | Opcode | Description |
| --- | --- | --- |
| **Data Movement** | | |
| LOAD | 0000 |  |
| STORE | 0001 |  |
| COPY | 0010 |  |
| **Logic Operations** | | |
| NOT | 0011 |  |
| OR | 0100 |  |
| AND | 0101 |  |
| **Arithmetic Operations** | | |
| ADD | 0110 |  |
| SUB | 0111 |  |
| MUL | 1000 |  |
| DIV | 1001 |  |
| REM | 1010 |  |
| **Branching** | | |
| CMP | 1011 |  |
| JMP | 1100 |  |
| JIE | 1101 |  |
| JINE | 1110 |  |
| **Halt Instruction** | | |
| HLT | 1111 |  |

**Flow of Control:**

For implicit control:

PC <- PC + 2

For branching statements: